- a logic control unit, having at least a pair of input/output ports for communicating with said parallel port;
- a memory unit for storing instructions for controlling said logic control unit and said computer and for temporary exchange of data; and an universal asynchronous [receiver/transmitter] combined receiver and transmitter; and
- a voltage converter for voltage interchange of RS-232 and TTL and enabling said logic control unit to communicate with said computer through said serial port and executing a [said] testing procedure by comparing input and output signals.

REMARKS

Claims 1-20, and 22 are now pending. Claim 1 is amended. No new matter is introduced.

Claims 1-4, 17-20 and 22 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended Claim 1, taking into suggestions made by the Examiner. Applicant respectfully submits that the amendment made to Claim 1 should remove the Examiner's 35 U.S.C. § 112, second paragraph, rejection. No new matter is introduced.

Applicant is also submitting as attached herewith a clean version of the Claims amended.

In light of the foregoing, it is believed that the present invention is in condition for allowance. An early and favorable action to that effect is respectfully solicited. If the Examiner has any question, he or she is invited to call or fax Applicant's counsel at the telephone numbers below.

Respectfully Submitted,

7/67/0

Date

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